

PCIe GEN4 SSD LEADER

PS5016 - E16

PCIe Gen4x4

Phison is proud to introduce the industry's first M.2 PCIe Gen 4x4 NVMe SSD. Evolving its award winning, high performance, PS5012-E12 design, the new PS5016-E16, with a PCIe Gen 4x4 front end, can reach groundbreaking speeds of 5GB/s sequential read and 4.4GB/s sequential write for a single M.2 device. This groundbreaking performance will give you access to your data faster, and provide you with the best user experience for your PC. With the next evolution of the PCI-Express interface ready for release, Phison will be the first and only company ready with a PCIe Gen 4x4 NVMe SSD solution.

The E16 is the result of Phison's decades of experience in memory technology, excellence in engineering, and innovation in flash memory products. Enabling the latest 96-layer 3D TLC NAND flash, the E16-based solutions offer capacities up to 2TB.



PCIe Gen 4x4

Fully compliant with PCI-Express 4.0, with a maximum throughput of 7.88 GB/s, the E16 can easily reach speeds of 5GB/s sequential reads and 4.4GB/s sequential writes, the fastest sequential reads and writes for a single M.2 SSD. It provides a 42% increase in sequential reads and 31% increase in sequential writes over the fastest Gen 3x4 SSD solution in the market.

Protecting your Data

Using Phison's 4th Generation LDPC ECC Engine, and fully integrated End-to-End data path protection, the E16 delivers an enhanced reliability for your SSD.

CONTROLLER

PS5016 - E16

Capacities	Max: 8TB	
PCIe	Speed & Lane #	Gen 4.0 x 4L
	NVMe Rev.	1.3
	Virtual Function	1
	Namespace	8
	Others	Boot Partition; RPMB
NAND	Channel #	Max: 8
	CE #	Max: 32
	Speed	Max: 800 MT/s per channel
DDR	DDR4 @ 1600, 16bit, 4 Rank, (2GB per rank)	
Performance <small>(BiCS4 32dies, 800MT/s)</small>	SR/SW (MBps)	Max: SLC: 5000/4400
	RR/RW (IOPS)	Max: 750K/750K ²
Power <small>(BiCS4 32dies, 800MT/s)</small>	SR (mW)	Typ: 3404
	SW (mW)	Typ: 3011
	Leakage @125°C (mW)	Max: 1100
Processor	32-bit ARM Cortex R5 (Two CPUs)	
	CoXProcessor Technology	
Peripheral Interface	Support of GPIO Pins, Build-in UART function, I2C and SPI for external ROM	
Data Reliability	4th Gen LDPC engine; End-To-End Data Path Protection; SmartECC (RAID ECC)	
SRAM Protection	TCM: 1-bit ECC, 2-bit EDC / Other SRAM: 1-bit EDC/parity	
Security	HW	AES 128/256 bit (XTS, CTR, CBC, ECB mode), SHA 160/256/512, RSA 2048
	FW	TCG Support & Opal 2.0, Pyrite, Sanitize and Crypto Erase
Temperature	Controller: -40 ~ 125°C (Tj)	
Others	Full Dynamic Range SLC cache support	
	4KB & 512B support	

1) Performance depends on host capability.

2) Performance is based on Intel Gen3 Z270 + PLDA Gen4 Switch

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THE DATA WITHIN THIS SPECIFICATION IS SUBJECT TO CHANGE BY PHISON WITHOUT NOTICE. PERFORMANCE NUMBERS MAY VARY BASED ON SYSTEM CONFIGURATION AND TESTING CONDITIONS.

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